REMARKS

Claims 1, 3, 5-9, 11-16, 18-21, and 23-31 are pending. Claims 1, 9, 16, and 21 are independent.

In the action mailed March 8, 2007, claims 11, 12, 18, and 23 were recognized as reciting allowable subject matter. Applicant acknowledges the recognition of allowable subject matter with appreciation.

Claim 1 was objected to as failing to properly establish antecedent basis for the recitation of "the processor." Claim 1 has been amended to address the Examiner's concerns.

Claim 1 and its dependencies were rejected under 35 U.S.C. § 101 as allegedly being directed to non-statutory subject matter. The rejection contends that "no concrete tangible results [are recited] for a possible outcome of the conditional claim." The rejection also contends that the final result of the claims is not a final tangible result "without clarification of what occurs when the instructions are invalid."

Applicant respectfully disagrees. Under 35 U.S.C. § 101, whoever invents or discovers any new and useful process or any improvement thereof may obtain a patent therefor. *See* 35 U.S.C. § 101. The fact that claim 1 and its dependencies do not recite what happens when instructions are invalid does not remove the

subject matter of claim 1 from the provisions of 35 U.S.C. § 101. In particular, claim 1 relates to a process regardless of whether the consequences of every possible outcome has been clarified in the claim.

Further, Applicant is unaware of any exception to 35 U.S.C. § 101—judicial or otherwise—that requires Applicant to recite what happens under every possible outcome of a process. Indeed, it defies logic to contend that a statutory process is somehow made unstatutory by unrecited subject matter.

Accordingly, claim 1 recites statutory subject matter. Applicant requests that the rejections of claim 1 and the claims dependent therefrom under 35 U.S.C. § 101 be withdrawn.

Rejections under 35 U.S.C. § 102(e)

Claim 9

Claim 9 was rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,070,252 to Xu et al. (hereinafter "Xu").

Claim 9 relates to a method of providing instructions to a processor. The method includes loading a plurality of instructions into an emulation instruction register from a test interface, receiving a run-test idle state signal, providing the plurality of instructions to a processor in response to the receipt of the run-test idle state signal, and processing the

plurality of instructions without receiving another run-test idle state signal. The run-test idle state signal indicates entry of the test interface into a run-test idle state.

As an anticipation rejection, the rejection of claim 9 is based on the contention that Xu shows the subject matter recited in claim 1 "in as complete detail as is contained in the ... claim." *See, e.g., M.P.E.P.* §2131 (*citing Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, (Fed. Cir. 1989)).

Applicant respectfully disagrees. In this regard, Xu is concerned with interactive built-in self-testing (BIST) with user-programmable test patterns. *See, e.g., Xu*, col. 3, line 32-34. Such interactive testing allows the user to modify a test pattern to, e.g., account for changes in memory cell layout, detect relatively uncommon faults, and pinpoint the location of certain errors. *Id.*, col. 3, line 23-35.

In order to achieve such interactive built-in self-testing, Xu describes that a BIST routine can begin with a check to determine whether a "DFU flag" is set. *Id.*, col. 4, line 57-60. If the DFU flag is not set, then the BIST routine runs using conventional fixed or random patterns. *Id.*, col. 4, line 60-62.

If the DFU flag is set, then the BIST routine determines whether a user-selected test pattern is available and performs the BIST using the user-provided pattern. *Id.*, col. 4, line 63-col. 5, line 2.

Perhaps because Xu is concerned with determining whether testing is to occur using conventional fixed or random patterns or with a user-selected test pattern, Xu does not provide many details regarding the actual BIST testing itself. For example, Xu neither describes nor suggests that a plurality of instructions that has been provided to a processor in response to receipt of a run-test idle state signal is processed without receiving another run-test idle state signal, as recited in claim 9.

The rejection of claim 9 contends that Xu, col. 6, line 4-63 describes otherwise. Applicant respectfully disagrees. In this regard, this portion of Xu describes a single four bit "private" instruction (denoted "BISTPAT") that sets the DFU flag *Id.*, col. 6, line 4-6. Once this single instruction has been latched, it becomes the current instruction. *Id.*, col. 6, line 17-18. Upon advancement to the RUN-TEST/IDLE state, the BISTPAT instruction is executed to set the DFU flag. *Id.*, col. 6, line 19-21.

After the DFU flag is set, the SHIFT-DR state is cycled through a predetermined number of cycles to serially read the user-provided test pattern into a test access port data register. *Id.*, col. 6, line 29-31. After the user-provided test pattern is latched in the data register, a flag that indicates that the user-provided test pattern is ready is asserted. *Id.*, col. 6, line 34-40. After the DFU flag and this flag have been set, the BIST routine can be invoked. *Id.*, col. 6, line 50-55.

Xu stops short of describing the details of the BIST routine. Instead, as discussed above, Xu is concerned with determining whether testing is to occur using conventional fixed or random patterns or with a user-selected test pattern.

Please note that Xu's processing of the single four bit "private" BISTPAT instruction also does describe nor suggest that a plurality of instructions that has been provided to a processor in response to receipt of a run-test idle state signal is processed without receiving another run-test idle state signal, as recited in claim 9. A single instruction is not a plurality of instructions. Moreover, there is no description or suggestion that this single instruction is somehow processed with other instructions without receiving another run-test idle state signal.

Accordingly, claim 9 is not anticipated by Xu. Applicant requests that the rejections of claim 9 and the claims dependent therefrom be withdrawn.

Claim 16

Claim 16 was rejected under 35 U.S.C. § 102(e) as anticipated by Xu.

Claim 16 relates to a processor that includes a test interface, an emulation instruction register adapted to store a plurality of emulation instructions received from the test interface, emulation control logic adapted to supply the plurality of emulation instructions to a processor pipeline in response to detection of an entry of the test interface into a run-test idle state, and a decoder to receive the plurality of instructions for processing.

Xu neither describes nor suggests emulation control logic that is adapted to supply a plurality of emulation instructions to a processor pipeline in response to detection of an entry of a test interface into a run-test idle state, as recited in claim 16.

In this regard, as discussed above, Xu is concerned with determining whether testing is to occur using conventional fixed or random patterns or with a user-selected test pattern. Xu does not provide many details regarding the actual BIST testing

itself. Moreover, Xu's processing of the single four bit "private" BISTPAT instruction does not describe or suggest that a plurality of emulation instructions is supplied to a processor pipeline in response to detection of an entry of a test interface into a run-test idle state, as the emulation control logic of claim 16 is adapted to do.

Accordingly, claim 16 is not anticipated by Xu. Applicant requests that the rejections of claim 16 and the claims dependent therefrom be withdrawn.

Claim 21

Claim 21 was rejected under 35 U.S.C. § 102(e) as anticipated by Xu.

Claim 21 relates to an apparatus that includes operating instructions residing on a machine-readable storage medium. The operating instructions are for use in a device to handle a plurality of emulation instructions. The operating instructions cause the device to load the plurality of emulation instructions into a single emulation instruction register, have a test interface enter a run-test idle state, provide the plurality of emulation instructions to a processor in response to entry of the test interface into the run-test idle state, and process the plurality of emulation instructions.

Xu neither describes nor suggests operating instructions that cause a device to provide a plurality of emulation instructions to a processor in response to entry of the test interface into the run-test idle state, as recited in claim 21.

In this regard, as discussed above, Xu is concerned with determining whether testing is to occur using conventional fixed or random patterns or with a user-selected test pattern. Xu does not provide many details regarding the actual BIST testing itself. Moreover, Xu's processing of the single four bit "private" BISTPAT instruction does not describe or suggest that a plurality of emulation instructions provided to a processor in response to entry of a test interface into a run-test idle state, as recited in claim 21. In this regard, a single BISTPAT instruction is not a plurality of emulation instructions.

Accordingly, claim 21 is not anticipated by Xu. Applicant requests that the rejections of claim 21 and the claims dependent therefrom be withdrawn.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue, or comment does not signify agreement with or concession of that rejection, issue, or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims

(or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Applicant asks that all claims be allowed. No fees are believed due at this time. Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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